

Description

METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING AIR GAPS AND THE STRUCTURE SO FORMED

BACKGROUND OF INVENTION

[0001] Technical Field

[0002] The present invention relates generally to semiconductor devices, and more particularly, to a method of forming a semiconductor device having air gaps within the wiring levels, and the structure so formed.

[0003] Related Art

[0004] As semiconductor devices continue to shrink, the distance between device features is reduced. Within metal wiring layers reducing the distance between features causes an increased capacitance. Therefore, there is a need in the industry for a method of forming a semiconductor device capable of maintaining a lower capacitance while reducing the distance between device features that overcomes the

above and other problems.

SUMMARY OF INVENTION

- [0005] The present invention provides a method of forming a semiconductor device having air gaps within the metal wiring level, and the structure so formed, that solves the above-stated problems.
- [0006] A first aspect of the invention provides a method of forming a semiconductor device, comprising: depositing alternating layers of a first and a second dielectric material, wherein the first and second dielectric materials are selectively etchable at different rates; forming a first feature within the alternating layers of dielectric material; and selectively etching the alternating layers of dielectric material to remove at least a portion, but not all, of the first dielectric material in each layer having the first dielectric material and leaving the second dielectric material as essentially unetched.
- [0007] A second aspect of the invention provides a method of forming a semiconductor device, comprising: depositing alternating layers of a first and a second insulative material; forming a damascene feature; and forming openings within the layers of first insulative material.
- [0008] A third aspect of the invention provides a semiconductor

device, comprising: semiconductor device, comprising: a metal wiring level having alternating layers of a first dielectric material and a second dielectric material having a first feature formed within the alternating layers of first and second dielectric material; and a plurality of openings within the first dielectric material.

[0009] A fourth aspect of the invention provides a semiconductor device, comprising: a plurality of alternating first and second insulative layers, wherein the first and second insulative layers have different etch rates; a first feature formed within the first and second insulative layers; a plurality of openings within the plurality of first insulative layers formed during a selective etch.

[0010] The foregoing and other features and advantages of the invention will be apparent from the following more particular description of the embodiments of the invention.

BRIEF DESCRIPTION OF DRAWINGS

[0011] The embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:

[0012] Fig. 1 depicts a cross-sectional view of a device comprising a pre-metal dielectric layer and a first insulative layer thereon, in accordance with embodiments of the present

invention;

[0013] Fig. 2 depicts the device of Fig. 1 having a second insulative layer thereon;

[0014] Fig. 3 depicts the device of Fig. 2 having a third insulative layer thereon;

[0015] Fig. 4 depicts the device of Fig. 3 having a fourth insulative layer thereon;

[0016] Fig. 5 depicts the device of Fig. 4 having a plurality of insulative layers thereon forming a first metal wiring level;

[0017] Fig. 6 depicts the device of Fig. 5 having a pair of damascene features formed therein;

[0018] Fig. 7 depicts the device of Fig. 6 having a plurality of air gaps formed within select insulative layers;

[0019] Fig. 8 depicts the device of Fig. 7 having a conformal liner formed thereover;

[0020] Fig. 9 depicts the device of Fig. 8 having a conductive layer deposited thereon;

[0021] Fig. 10 depicts the device of Fig. 9 following polishing;

[0022] Fig. 11 depicts the device of Fig. 10 having an insulative layer formed over the first metalwiring level;

[0023] Fig. 12 depicts the device of Fig. 11 having a plurality of insulative layers forming a second metal wiring level;

[0024] Fig. 13 depicts the device of Fig. 12 having a first dama-

scene feature formed therein;

[0025] Fig. 14 depicts the device of Fig. 13 having second damage scene features formed therein;

[0026] Fig. 15 depicts the device of Fig. 14 having a plurality of air gaps formed within select insulative layers;

[0027] Fig. 16 depicts the device of Fig. 15 having a conductive layer deposited thereon; and

[0028] Fig. 17 depicts the device of Fig. 16 following polishing.

DETAILED DESCRIPTION

[0029] Although certain embodiments of the present invention will be shown and described in detail, it should be understood that various changes and modifications might be made without departing from the scope of the appended claims. The scope of the present invention will in no way be limited to the number of constituting components, the materials thereof, the shapes thereof, the relative arrangement thereof, etc. Although the drawings are intended to illustrate the present invention, the drawings are not necessarily drawn to scale.

[0030] Fig. 1 depicts a cross-sectional view of a pre-metal dielectric (PMD) 10 upon which a first insulative layer 12a is formed. The PMD 10 comprises one or more dielectric

materials, such as a SiO_2 -based material, i.e., SiO_2 , PSG, BPSG, SiCOH (OSG), SILKTM (Dow Chemical Corp.), SiN, SiC, SiCN, C-H, etc. The first insulative layer 12a comprises a dielectric material, in this example, an organic dielectric material, such as, polyarylene ether (SILKTM), parylene (N or F), Teflon, or other porous versions of these films. The type of organic dielectric material used may depend upon the deposition technique used. For example, if the first insulative layer 12a is formed using chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD), the parylene (N or F), Teflon, or other porous versions of these films may be used. If, however, first insulative layer 12a is formed using spin-on deposition, the SILKTM may be used. The first insulative layer 12a may be formed having a thickness within the range of 5–10 nm.

[0031] A second insulative layer 14a is then formed on the first insulative layer 12a, as illustrated in Fig. 2. The second insulative layer 14a comprises a dielectric material, in this example, an inorganic dielectric material, such as, SiCOH (OSG), SiO_2 , fluorinated SiO_2 (FSG), such as methylsilesquoxane (MSQ), or porous versions of these materials. As with the first insulative layer 12a, the second insulative

layer 14a may be formed using CVD, PECVD, spin-on deposition, or other similar deposition techniques. The second insulative layer 14a may be formed having a thickness within the range of 5–10 nm.

[0032] As illustrated in Fig. 3, a third insulative layer 12b is formed on the second insulative layer 14a. The third insulative layer 12b comprises an organic dielectric material similar to that of the first insulative layer 12a. The third insulative layer 12b is formed using similar techniques, and having a similar thickness, to that of the first insulative layer 12a.

[0033] As illustrated in Fig. 4, a fourth insulative layer 14b is formed on the third insulative layer 12b. The fourth insulative layer 14b comprises an inorganic dielectric material similar to that of the second insulative layer 14a. The fourth insulative layer 14b is formed using similar techniques, and having a similar thickness, to that of the second insulative layer 14a.

[0034] Alternating layers of organic and inorganic dielectric material may be formed in this manner on the substrate 10, as illustrated in Fig. 5, to a desired thickness for a first metal wiring level 20. In the present example layers 12c–12f comprise an organic dielectric material similar to

that of the first and third insulative layers 12a, 12b. Likewise, layers 14c–14f comprise an inorganic dielectric material similar to that of the second and fourth insulative layers 14a, 14b. The number of layers depicted in the present invention is for illustrative purposes only, and is not intended to be limiting in any way, so long as at least one organic layer and one inorganic layer are present. Also, it should be noted that the organic dielectric material is deposited first in the present example for illustrative purposes only. Either the inorganic or organic dielectric material may be deposited first.

[0035] It should also be noted that it may be desirable to deposit the alternating layers of organic and inorganic insulative material in-situ. For example, a single PECVD chamber may be used to deposit both the inorganic and organic layers without leaving the chamber. Also, a spin-apply track may be used wherein the alternating layers are both deposited and cured within the same chamber. Using either technique, the first insulative layer 12a may alternatively be deposited having twice the desired thickness. Thereafter, the first insulative layer 12a is exposed to a plasma or thermal treatment wherein an upper portion of the first insulative layer 12a is converted into the material

needed in the second insulative layer 14a. These methods may help to decrease unevenness in thickness between the organic and inorganic insulative layers, and may increase adhesion between the organic and inorganic insulative layers.

[0036] As illustrated in Fig. 6, after the desired thickness for the first wiring level 20 has been achieved, a first feature 22 and, in this example, a second feature 24, are formed within the first wiring level 20. The first and second features 22, 24 are wire trenches for wiring lines that may be formed using conventional patterning and etching techniques.

[0037] Following formation of the first and second features 22, 24, a selective etch is performed to remove at least portions of the organic dielectric material within the first wiring level 20, in this example, within layers 12a-12f (Fig. 7). In the present example, where the organic dielectric material comprises p-SILKTM and the inorganic dielectric material comprises p-OSG, an N₂ plasma, H₂ plasma, or other similar plasma etch may be used to selectively remove the organic dielectric material. The N₂ or H₂ etch may be operated in a pressure range of about 3-200 mT at typical parallel plate or high density plasma power and

flow conditions. Alternatively, portions of the inorganic dielectric material (p-OSG) may be etched using a wet etchant, such as a 100:1 DHF, leaving the SiLKTM material within layers 14a-14f.

[0038] As illustrated in Fig. 7, openings or air gaps 26 are formed following the selective etch of the organic dielectric material within layers 12a-12f. The air gaps 26 are formed within the organic dielectric material of layers 12a-12f, and not within the inorganic dielectric material within layers 14a-14f, because the etch rate of the organic dielectric material of layers 12a-12f is faster than the etch rate of the inorganic dielectric material of layers 14a-14f. The air gaps 26 within the first wiring level 20 reduce the capacitance within the overall device. The size of the air gaps 26 is determined by calibrating the selective etch to remove a portion, but not all, of the organic dielectric material. At least some of the organic dielectric material should remain after the selective etch to prevent mechanical failure of the device, e.g., collapse of the inorganic dielectric layers 14a-14f.

[0039] Table 1 below shows estimated comparisons of the capacitance value of the device, using different organic and inorganic materials, with and without the air gaps 26. In

particular, the data is modeled from a sample having a first wiring level 20 wire width of about 100nm and a wire spacing of about 100nm, wherein about 33nm of the 100nm organic dielectric within the wire spacing has been removed. This results in about a 20% reduction in K_{eff} (the effective dielectric constant of the device), which translates into about a 20% reduction in the capacitance of the device, since K_{eff} is proportional to the capacitance of the device.

Table 1: Comparison of K_{eff} with air gaps and K_{eff} without air gaps.

Inorganic Dielectric	Organic Dielectric	K_{eff} no air gaps	K_{eff} with air gaps	% reduction in K_{eff}
SiO_2 ($K=4$)	$SiLK(K=2.6)$	3.30	2.70	18%
$SiCOH$ ($K=3$)	$SiLK(K=2.6)$	2.80	2.24	20%
$p-SiCOH^*(K=2.5)$	$SiLK(K=2.6)$	2.55	1.99	22%
$p-SiO_2^*(K=2)$	$p-SiLK^*(K=2.2)$	2.10	1.68	20%

(* The "p-" indicates that the dielectric is a porous dielectric.)

[0040] After the air gaps 26 are formed, the surface 28 of the first metal wiring layer 20 is sealed to prevent metal, deposited in the next step, from leaking into the air gaps 26. This may be accomplished in several different ways. For example, a conformal liner 30, such as a dielectric having a low dielectric constant, i.e., $SiCOH$, SiO_2 , SiN , SiC , and $SiCN$, etc., is deposited over the surface 28 of the first metal wiring layer 20 (Fig. 8). The liner 30 may be deposited, having a thickness in the range of about 1–10nm,

using PECVCD, HDPCVD, SACVD, APCVD, THCVD, or other similar deposition techniques.

[0041] Alternatively, if the air gaps 26 are small, e.g., in the range of about 1–10nm, the metal deposited in the following step may be sufficient to seal the air gaps 26. A plasma vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), or other similar deposition technique may also be used to deposit the metal such that very few metal ions actually penetrate the air gaps 26.

[0042] After the air gaps 26 are sealed, if a separate sealing process is used as described supra, a conductive material 32 is deposited over the surface 28 of the first wiring level 20 filling the first and second features 22, 24 (Fig. 9). The conductive material 32 may comprise copper lined with a thin refractory metal liner, such as tantalum, as known in the art, or other similarly used material. The surface 28 of the first wiring level 20 is polished, using conventional techniques, to remove the excess conductive material 32, leaving the conductive material 32 within the first and second features 22, 24 to form a first wire 34 and a second wire 36 (Fig. 10).

[0043] The first metal wiring level 20 illustrated in this example

is a single damascene wiring level. As illustrated in Figs. 11–17, the present invention is designed for use in conjunction with a dual damascene wiring level as well. As shown in Fig. 11, a third insulative layer 38 may be deposited over the surface 28 of the first wiring level 20. The third insulative layer 38 may comprises one or more dielectric materials, having a low dielectric constant, that is not susceptible to removal during the subsequent etch process used to form the air gaps (formed infra). For example, the third insulative layer 38 may comprise porous SiCOH (p-OSG), SiO₂, fluorinated SiO₂ (FSG), SiCOH (OSG), such as methylsilesquoxane (MSQ), or porous versions of all these materials. The third insulative layer 38 may be formed using CVD, PECVD, spin-on deposition, or other similar deposition techniques, and may consist of multiple layers, such as SiN, SiC, FSG, etc. The third insulative layer 38 may be formed having a thickness approximately equal to the final via height, e.g., 0.1 to 1.0 micron.

[0044] Alternating layers of organic dielectric material 40a–40f and inorganic dielectric material 42a–42f are deposited on the surface 40 of the third insulative layer 38, as shown in Fig. 12, to form a second wiring level 50. The alternating layers are similar to those formed in the first metal wiring

level 20 (that is, organic dielectric material, inorganic dielectric material, organic dielectric material, inorganic dielectric material, etc.), and are formed in a similar manner.

[0045] After the second wiring level 50 is formed, a first dual damascene feature 44 is formed within the alternating layers of inorganic dielectric material 40a–40f, organic dielectric material 42a–42f, and the third insulative layer 38. As illustrated in Fig. 13, the first dual damascene feature 44 is a via trench. The via trench 44 is formed down to the first metal wiring level 20 using conventional patterning and etching techniques.

[0046] As illustrated in Fig. 14, a second dual damascene feature 46 and a second trench 48 are formed within the alternating layers of organic dielectric material 40a–40f and inorganic dielectric material 42a–42f. The second dual damascene feature 46 is also a wire trench formed, using conventional patterning and etching techniques, down to the surface of the third insulative layer 38. Alternatively, a trench first–via second process, as known in the art, may be employed. Likewise, a multi–layer hardmask may be used, in which the first damascene feature is patterned and etched into the upper hardmask, as known in the art.

[0047] After the first and second dual damascene features 44, 46, 48 are formed, a selective etch is performed to remove at least portions of the organic dielectric material 40a-40f within the second wiring level 50. As described above, where the organic dielectric material comprises p-SILKTM and the inorganic dielectric material comprises p-OSG, an N₂ plasma, H₂ plasma, or other similar plasma etch may be used to selectively remove the organic dielectric material. The N₂ or H₂ etch may be operated in a pressure range of about 3-200 mT at typical parallel plate or high density plasma power and flow conditions.

[0048] As illustrated in Fig. 15, openings or air gaps 52 are formed within the second wiring level 50 following the selective etch. It should be noted that no air gaps 52 are formed in the third insulative layer 38 of the present example to add mechanical strength and stability to the overall device. A conformal liner 53 is then formed on the surface of the second metal wiring level 50 sealing the second metal wiring level 50 to prevent metal, deposited in the next step, from leaking into the air gaps 52.

[0049] A conductive material 54 is deposited over the surface of the second wiring level 50 filling the via trench 44 and trenches 46, 48 (Fig. 16). The conductive material 54 may

comprise copper lined with a thin refractory metal liner, e.g., tantalum, or other similarly used material. The surface of the second wiring level 50 is polished, using conventional techniques, to remove the excess conductive material 54, leaving the conductive material 54 within the via trench 44 and wire trenches 46, 48 to form a conductive dual damascene feature 60 and a conductive single damascene feature 62 (Fig. 17).

[0050] Formation of air gaps within the metal wiring levels of the present invention provides a decreased overall capacitance of the device. This is particularly helpful as devices become smaller and smaller, and the distance between device features continues to decrease.